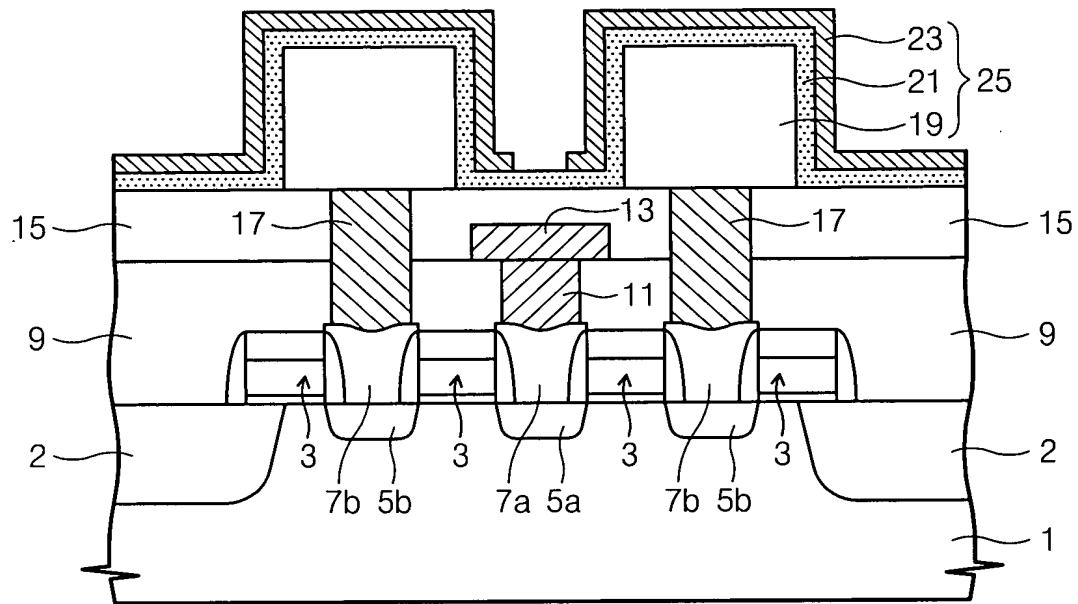


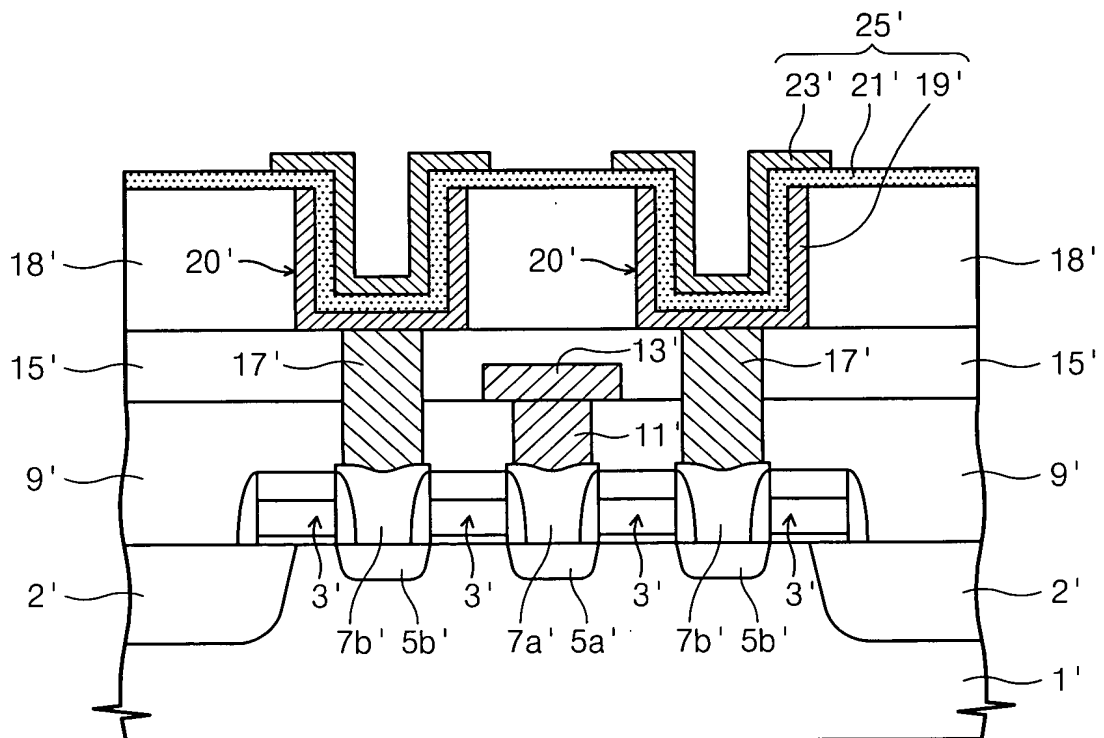
# Fig. 1

(PRIOR ART)

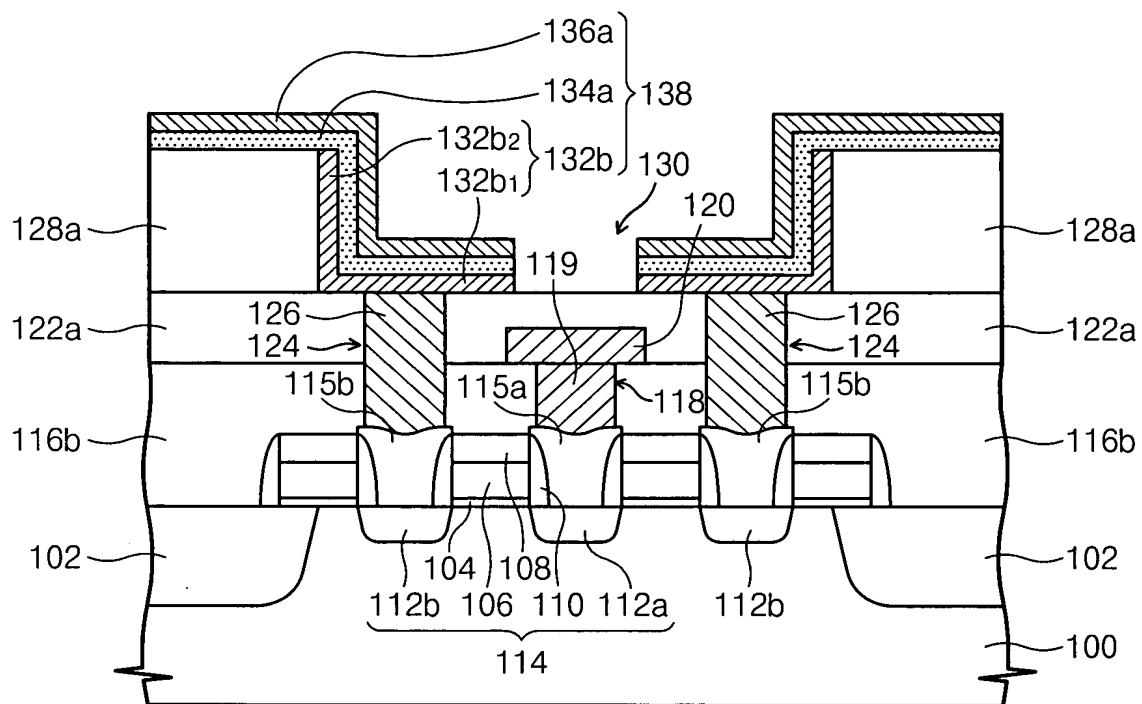


# Fig. 2

(PRIOR ART)



**Fig. 3**



**Fig. 4**

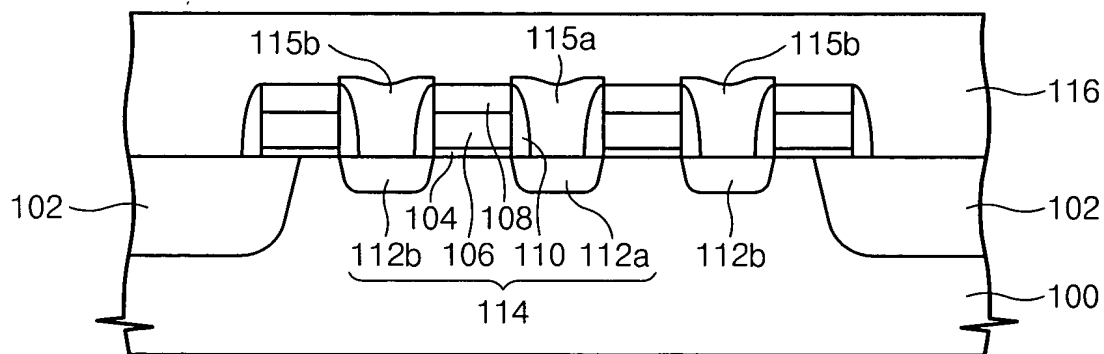


Fig. 5

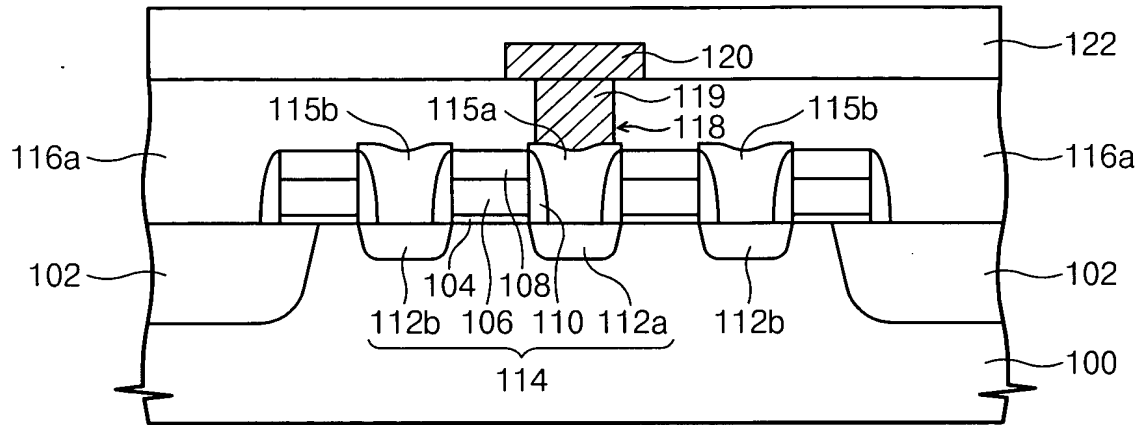


Fig. 6

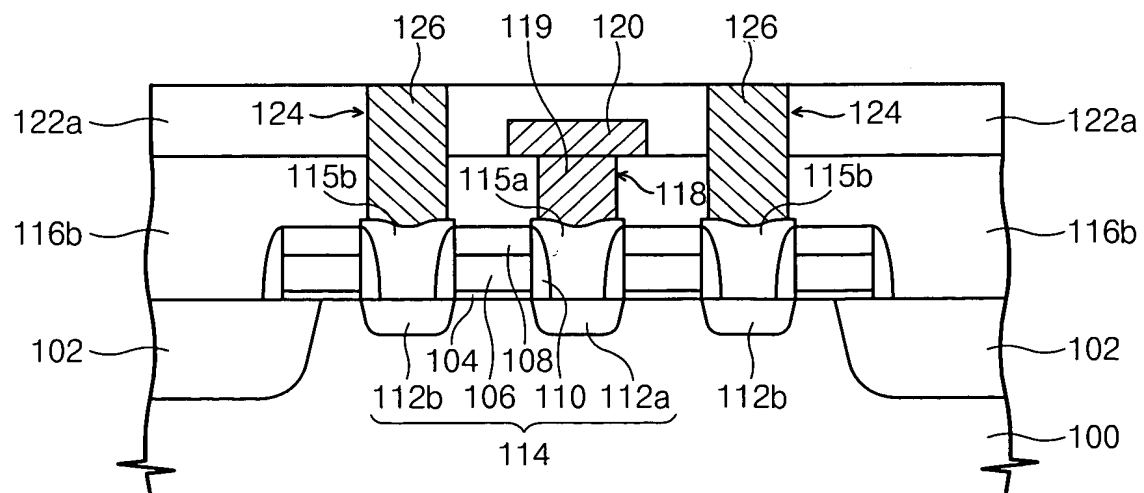


Fig. 7

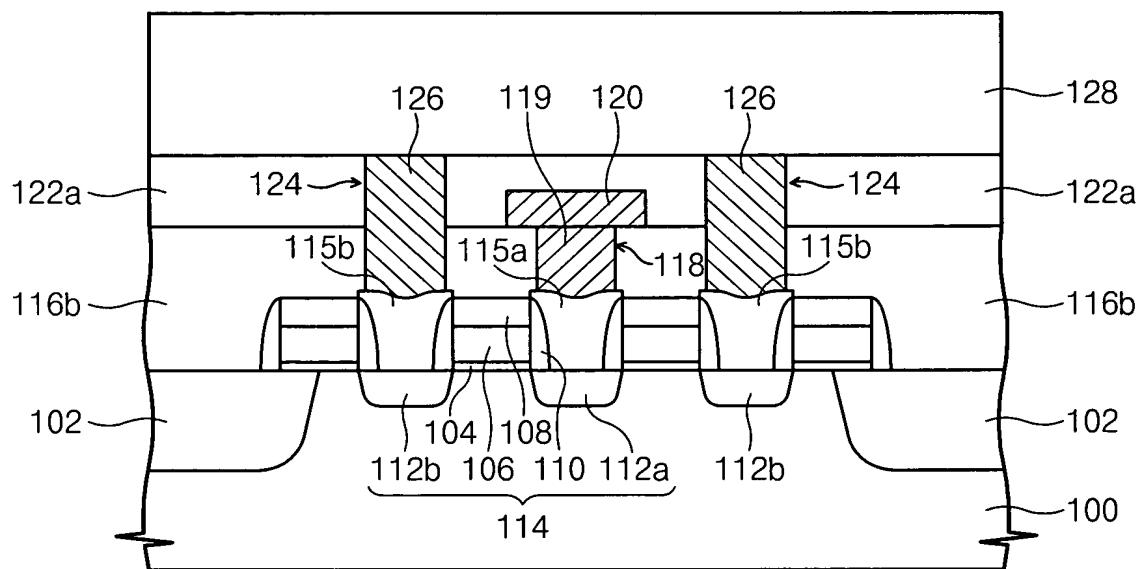


Fig. 8

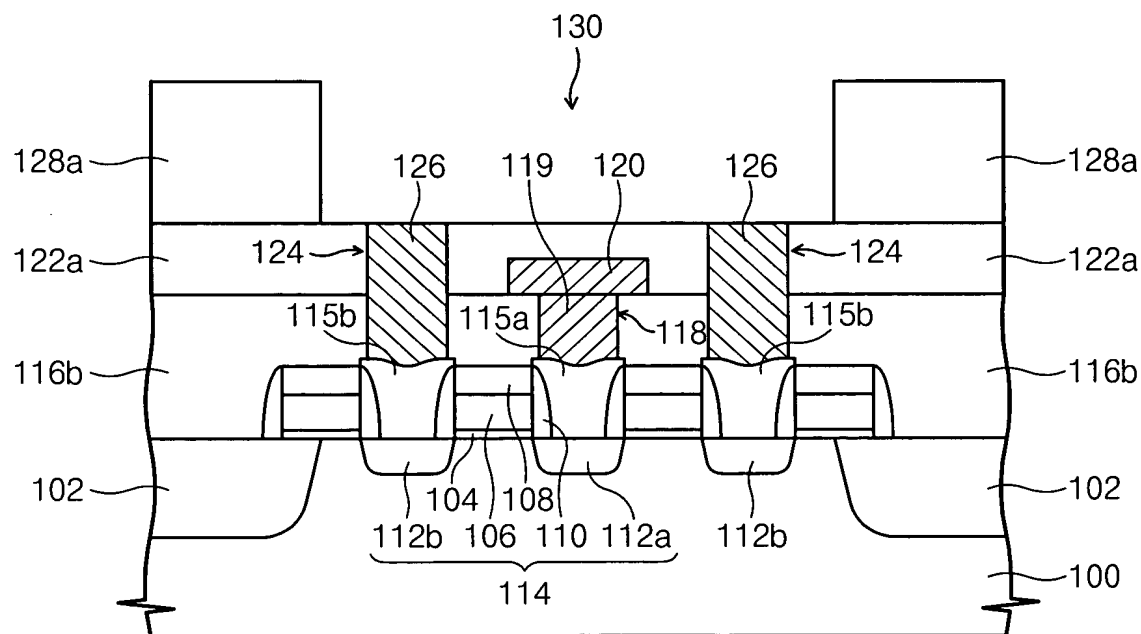


Fig. 9

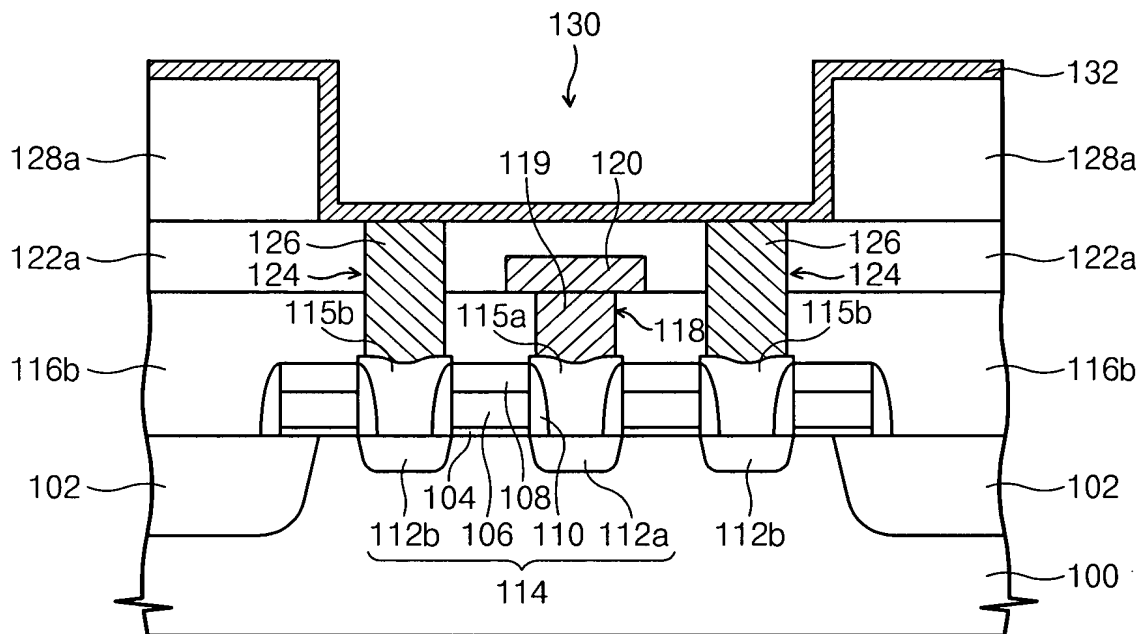


Fig. 10

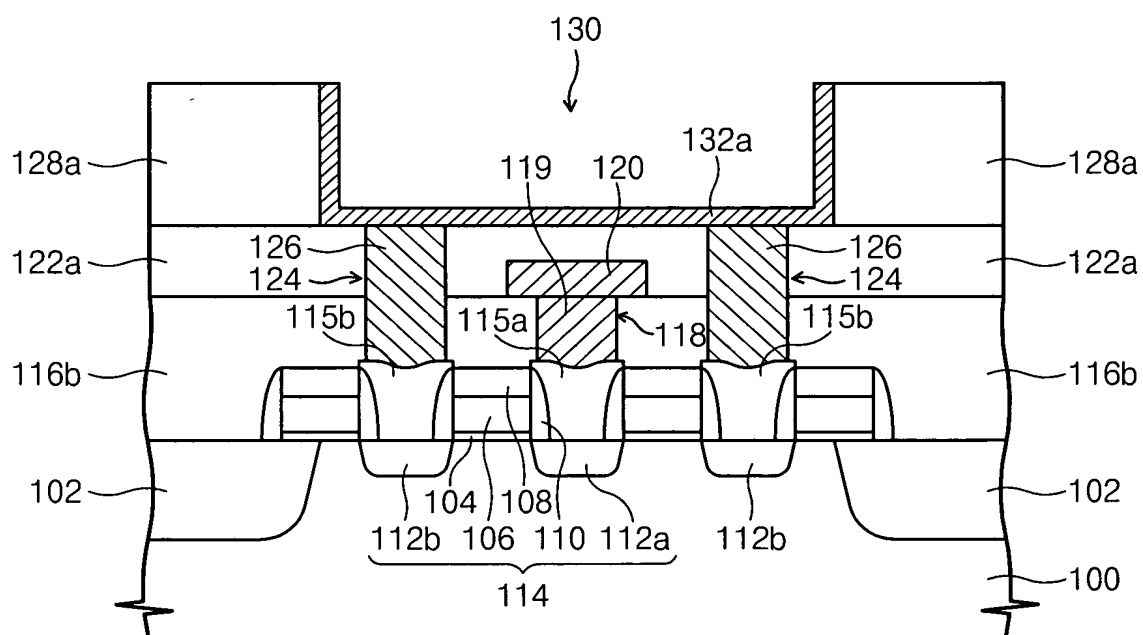


Fig. 11

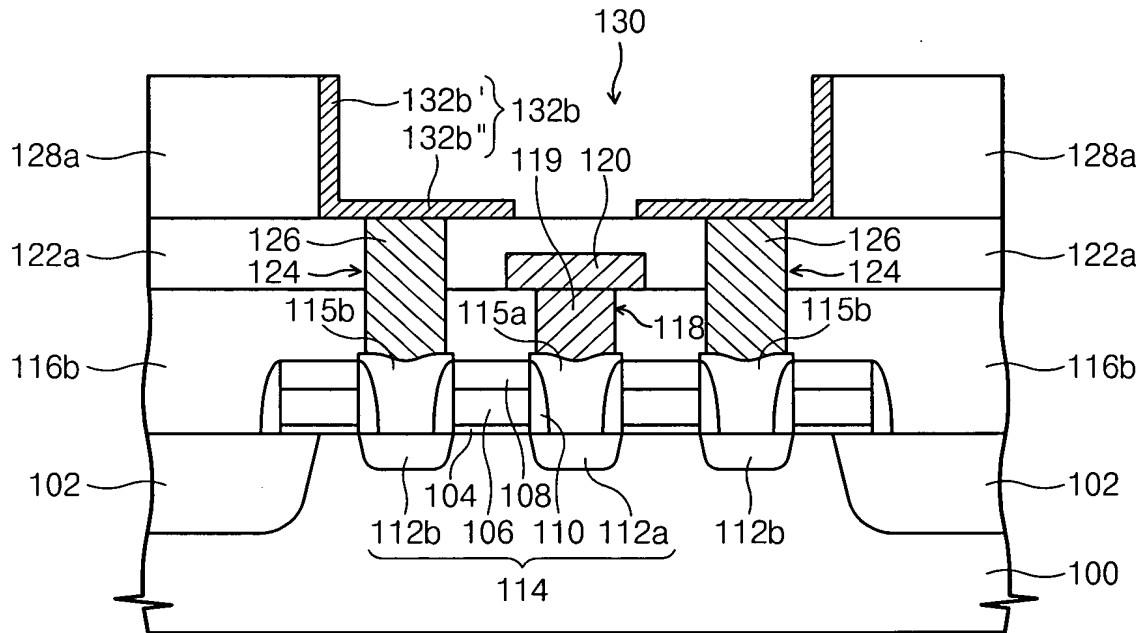


Fig. 12

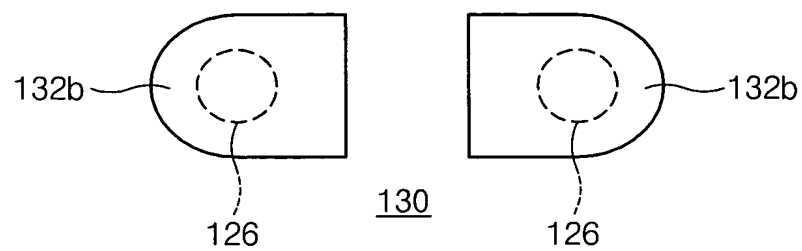


Fig. 13

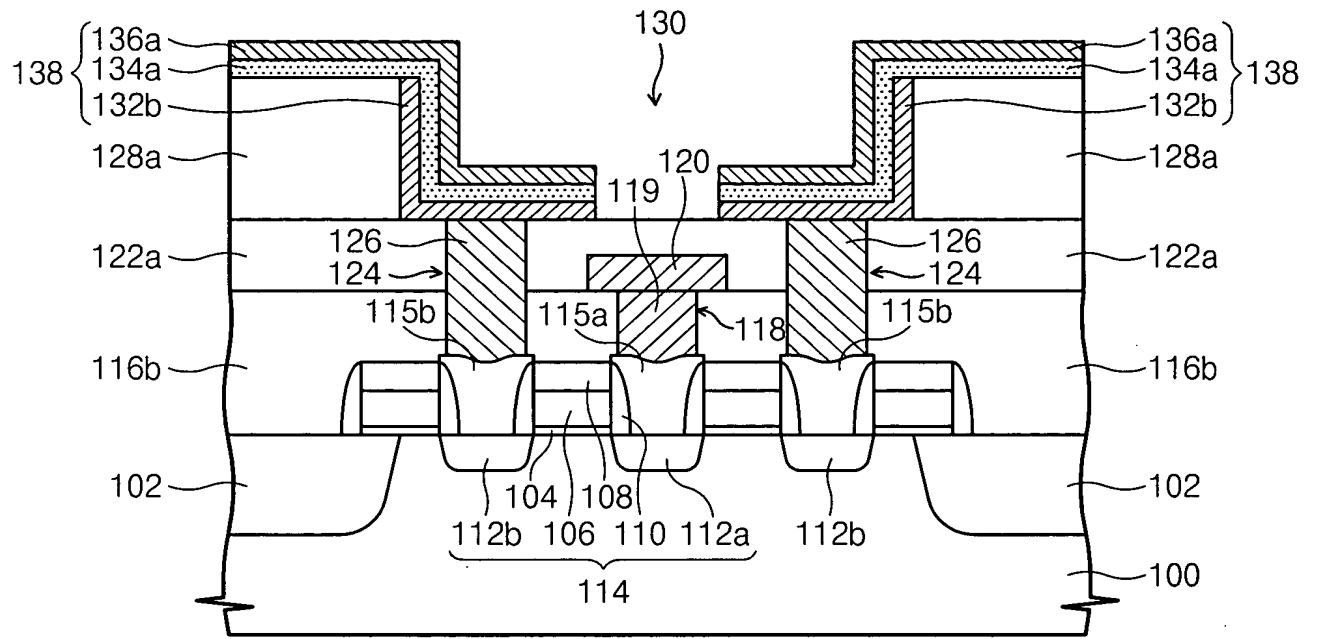


Fig. 14

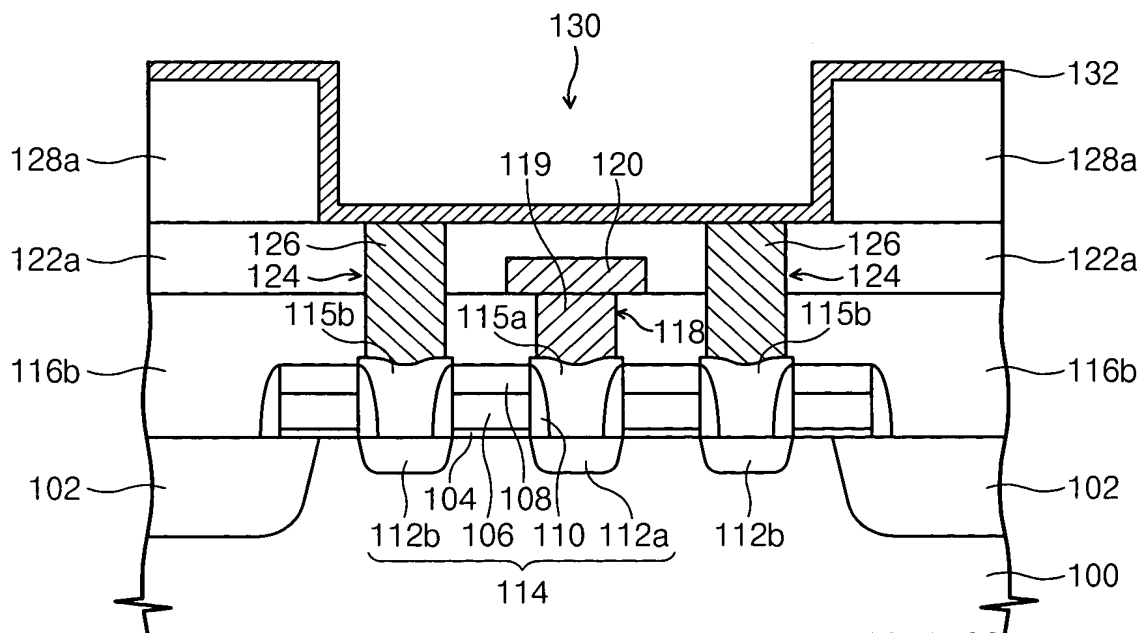


Fig. 15

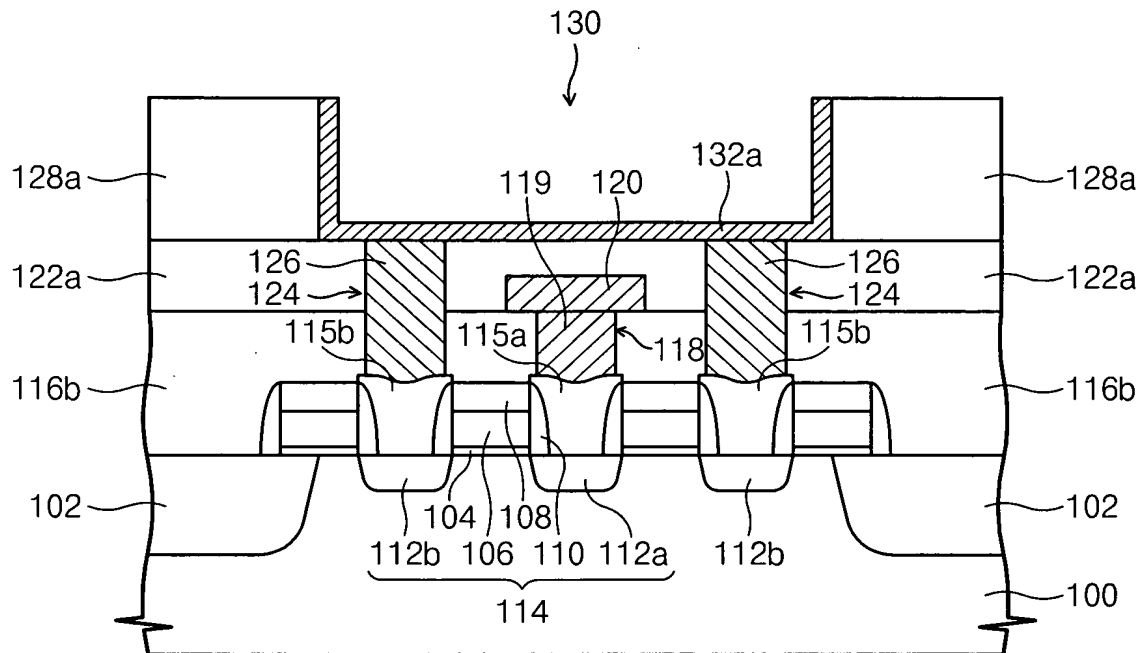
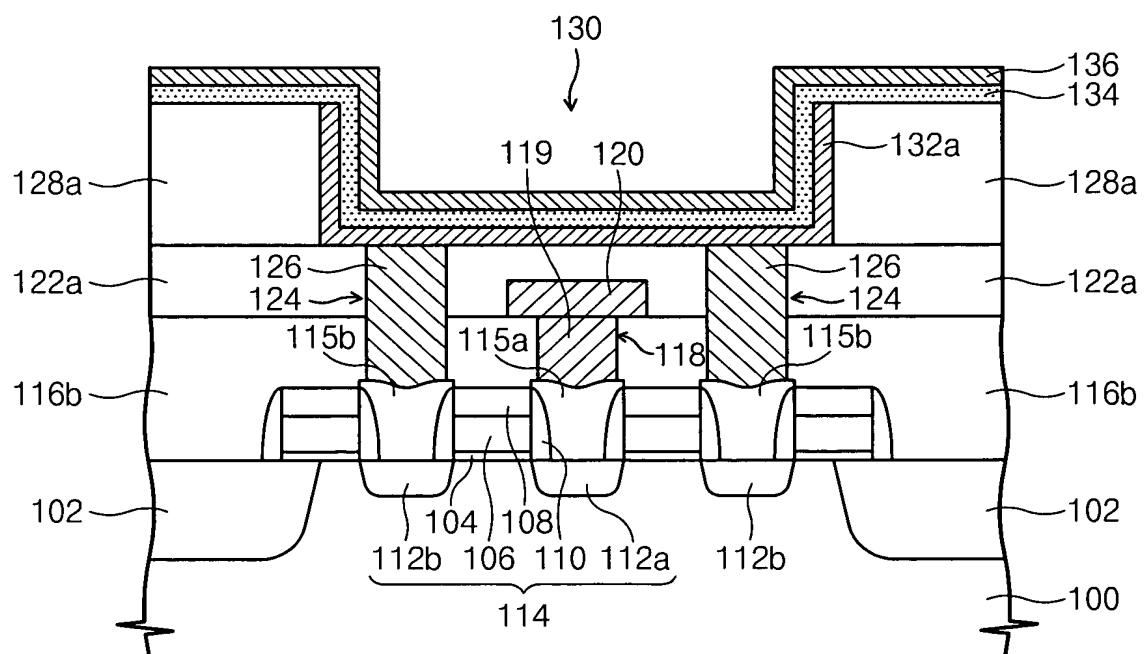


Fig. 16







A cross-sectional view of a semiconductor device. A substrate 200 is shown at the bottom. A channel region 202 is formed in the substrate. A series of gate electrodes 215a and 215b are positioned above the channel region. The gate electrodes are separated by gate spacers 212a and 212b. The gate spacers 212a and 212b are formed on the side walls of the gate electrodes. The gate electrodes 215a and 215b are connected to a common gate line 204. The gate line 204 is connected to a common gate terminal 206. The gate electrodes 215a and 215b are connected to a common gate terminal 208. The gate electrodes 215a and 215b are connected to a common gate terminal 210. The gate electrodes 215a and 215b are connected to a common gate terminal 212a. The gate electrodes 215a and 215b are connected to a common gate terminal 212b. The gate electrodes 215a and 215b are connected to a common gate terminal 214.

This cross-sectional view shows a semiconductor device with a central gate stack and side gates. The central gate stack includes a gate dielectric layer 219, a gate electrode 220, and a gate spacer 226. The side gates consist of a gate dielectric layer 215b and a gate electrode 215a. The device is formed on a substrate 202, which is connected to a ground potential 200. The central gate stack is connected to a power supply 204. The side gates are connected to a power supply 206. The device includes a channel region 210, a source region 212a, and a drain region 212b. The side gates are positioned on the sides of the channel region and source/drain regions. The gate dielectric layer 215b is located on the top surface of the side gates. The gate electrode 215a is located on the top surface of the side gates. The gate spacer 226 is located on the top surface of the central gate stack. The gate dielectric layer 219 is located on the top surface of the central gate stack. The gate electrode 220 is located on the top surface of the central gate stack. The gate spacer 226 is located on the top surface of the central gate stack. The device is formed on a substrate 202, which is connected to a ground potential 200. The central gate stack is connected to a power supply 204. The side gates are connected to a power supply 206. The device includes a channel region 210, a source region 212a, and a drain region 212b. The side gates are positioned on the sides of the channel region and source/drain regions. The gate dielectric layer 215b is located on the top surface of the side gates. The gate electrode 215a is located on the top surface of the side gates. The gate spacer 226 is located on the top surface of the central gate stack. The gate dielectric layer 219 is located on the top surface of the central gate stack. The gate electrode 220 is located on the top surface of the central gate stack. The gate spacer 226 is located on the top surface of the central gate stack.

Fig. 22

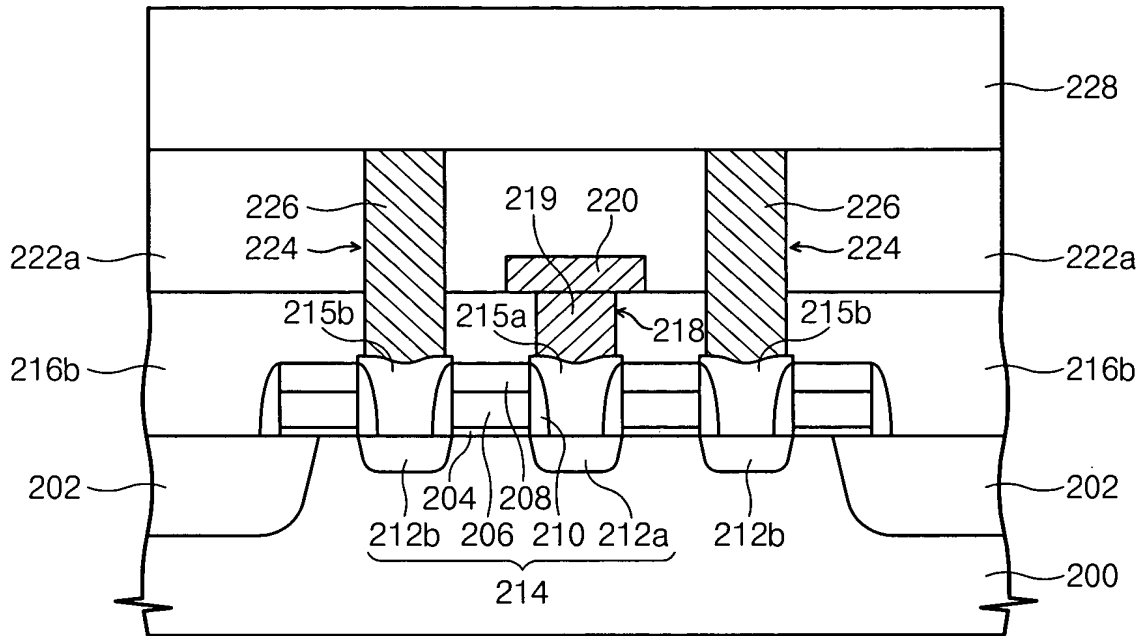
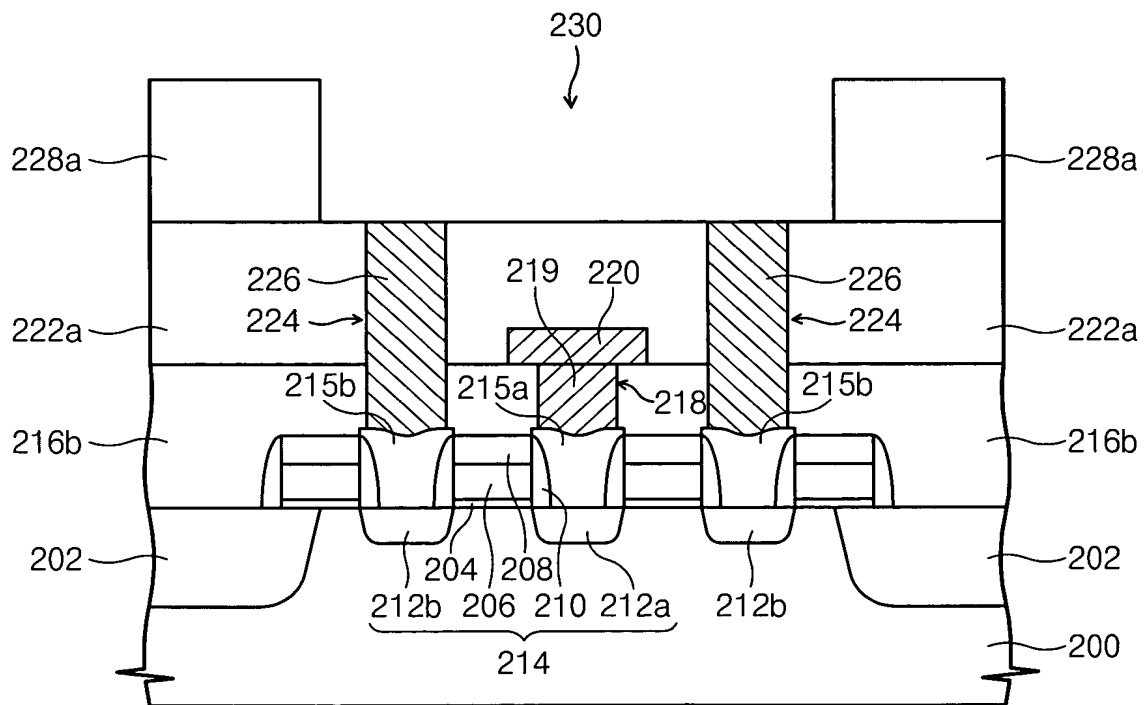


Fig. 23



A cross-sectional view of a semiconductor device 230a. The device is built on a substrate 200. A base layer 202 is formed on the substrate. On top of the base layer, there are several layers and structures. A layer 216b is formed, followed by a layer 215b. A central region 214 is defined, containing a structure 218. This structure 218 is surrounded by a layer 215a. Above the central region, there is a layer 220. The entire structure is covered by a layer 224. The top surface of the device is labeled 228a. The device is shown in a cross-section with a central channel or gap.

Fig. 26

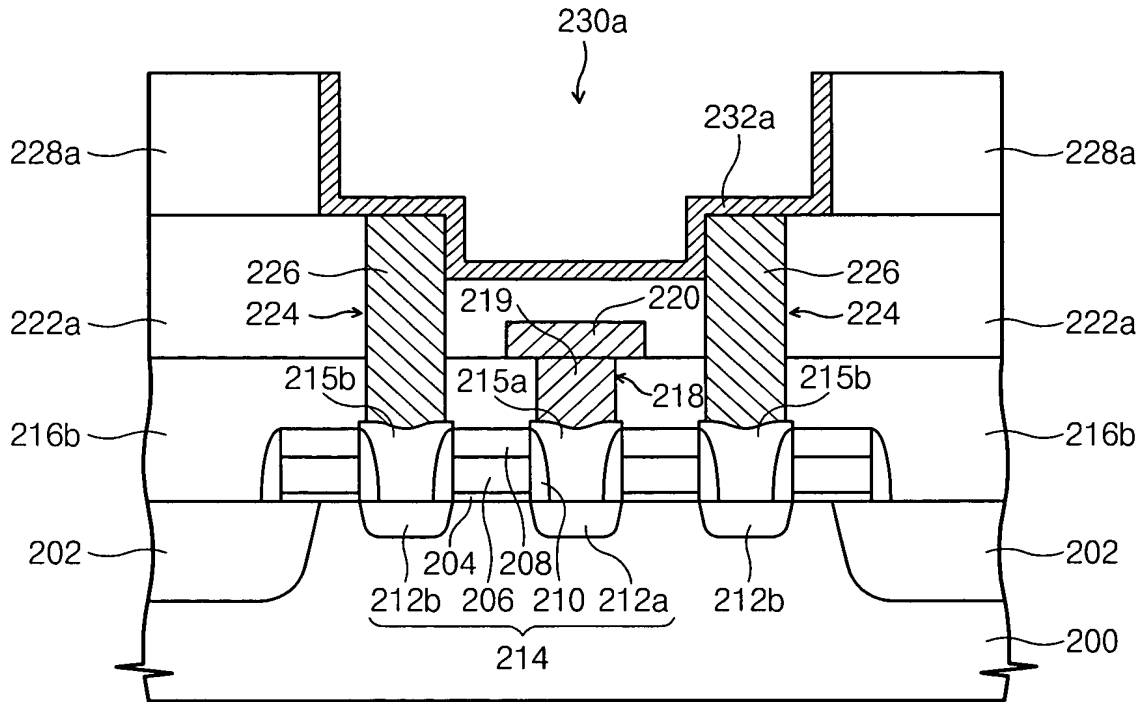


Fig. 27

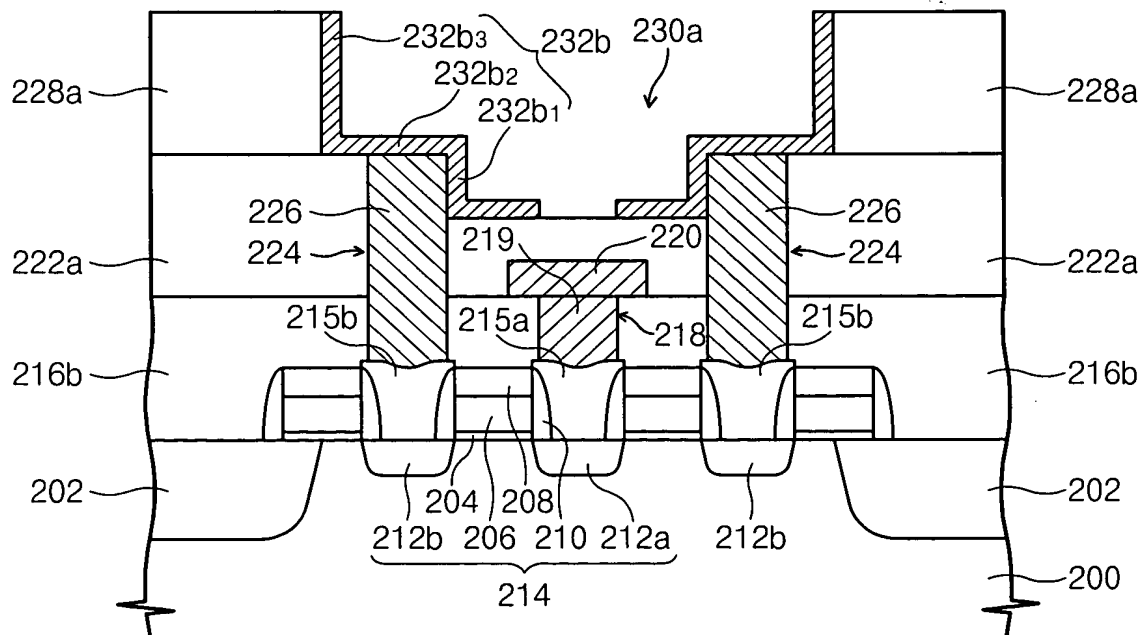


Fig. 28

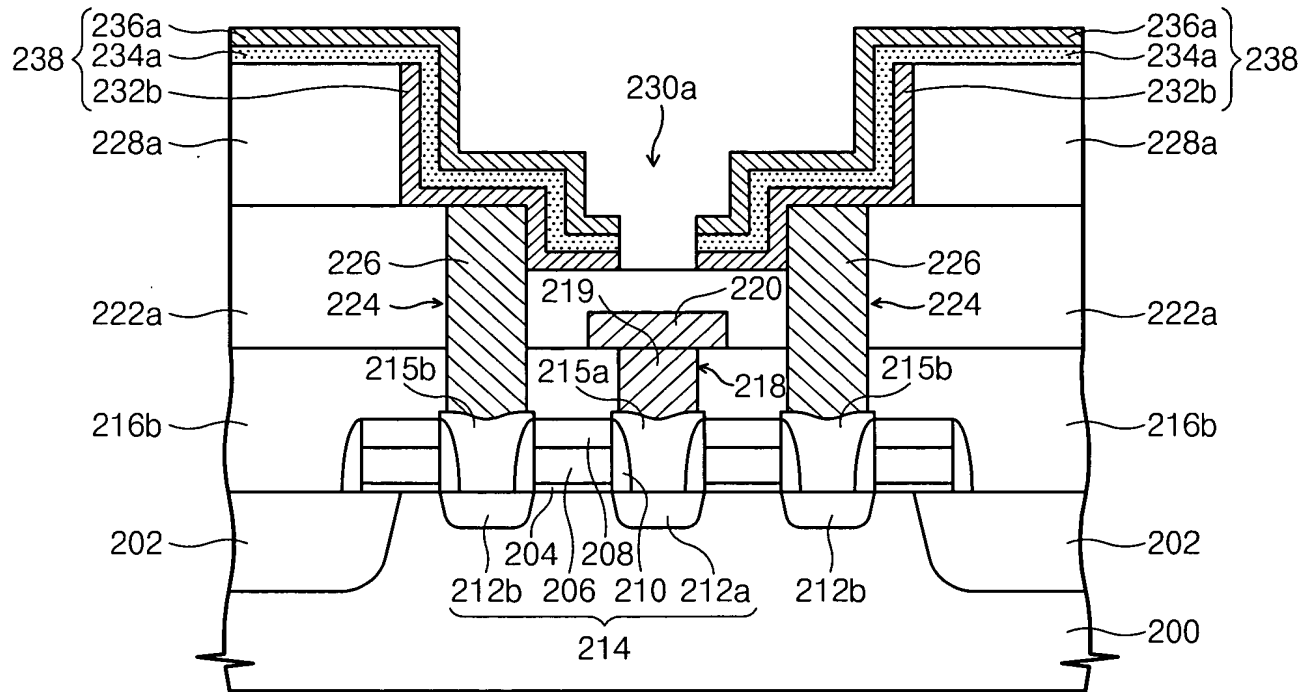


Fig. 29

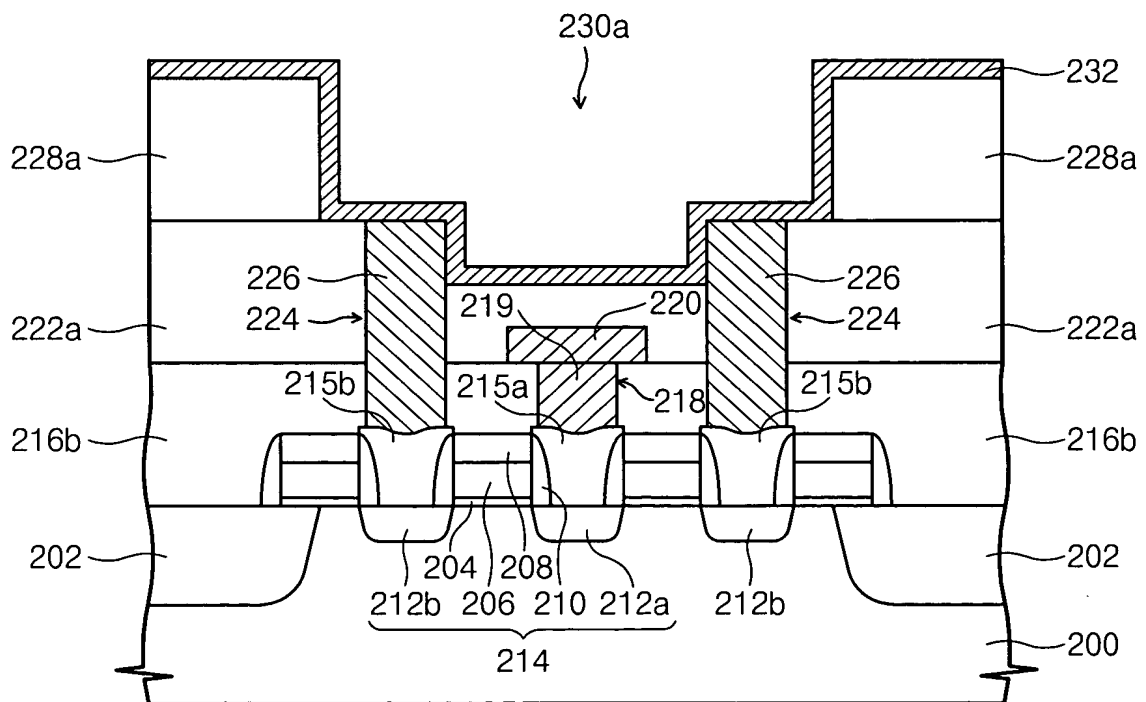


Fig. 30

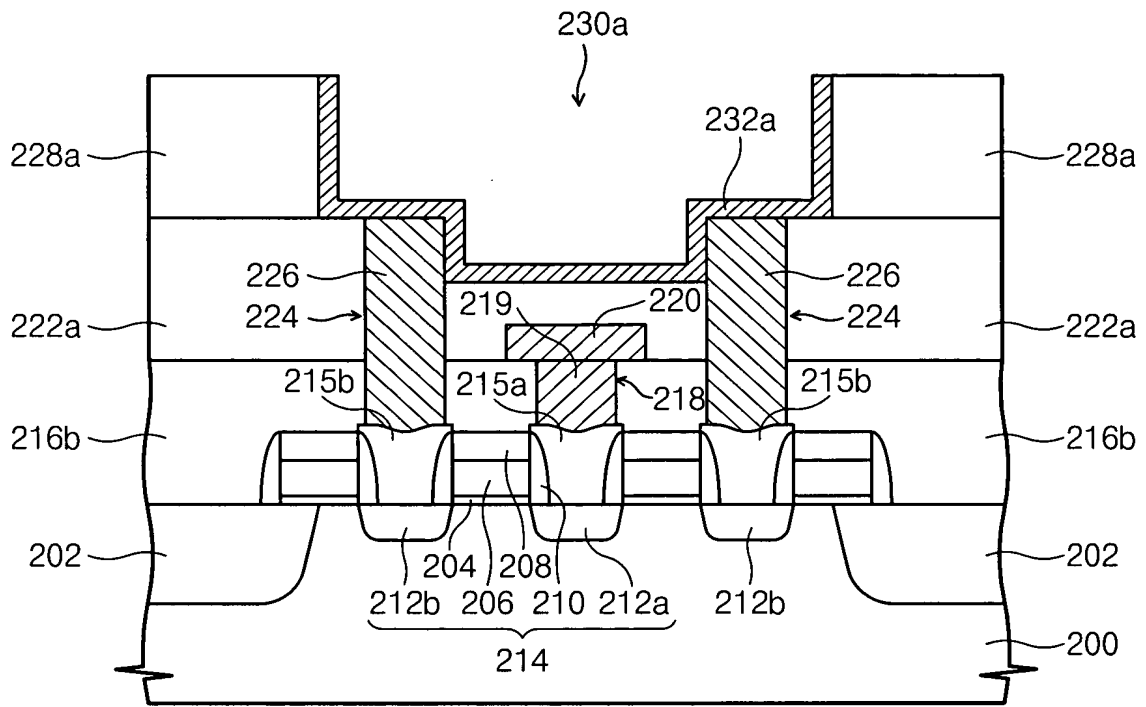


Fig. 31

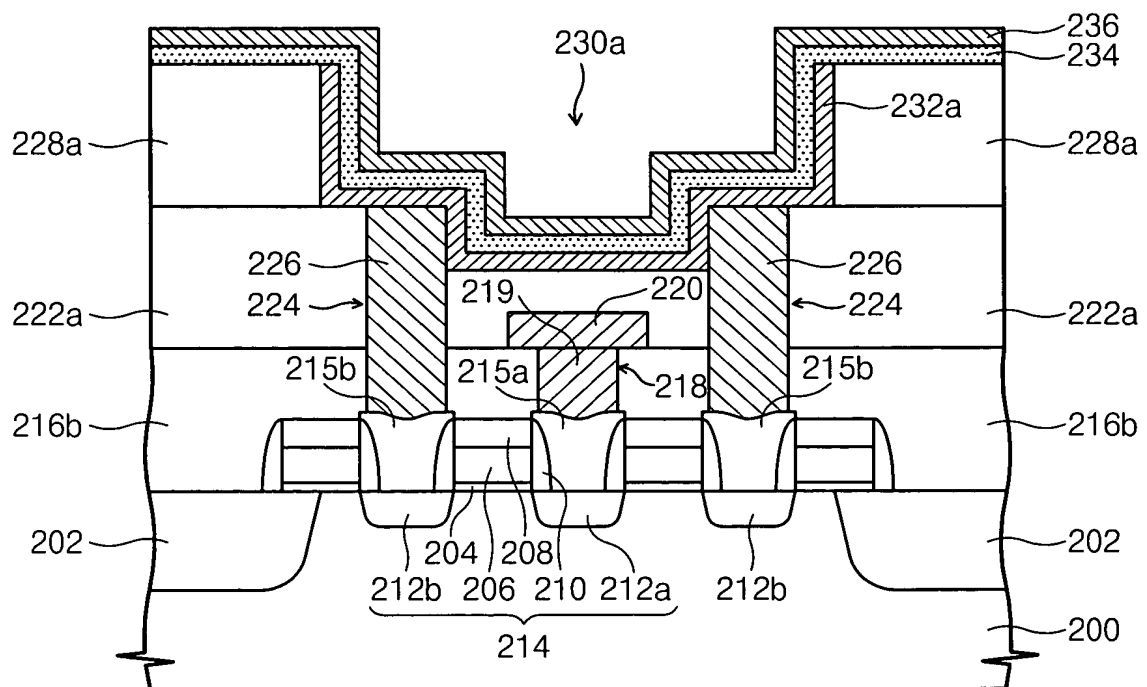


Fig. 32

